certain level. The manufacturer can assign other macro-cells to the vacancies (for example, as illustrated in Figure 21 by macro-cell 24 positioned in a vacancy in peripheral area 1b of device 1). Thus, any real estate is not wasted.

IN THE CLAIMS

Please amend claims 1, 2, 3, and 11 as follows:

1. (Amended) A flip chip semiconductor device of a multiplexing-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged in an area outside of an area of said power supply pads.

2. (Amended) A flip chip semiconductor device of a multi-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged outside of said power supply pads;

in which said signal pads and said power supply pads are to be connected to corresponding signal pads directly connected to signal lines without passing through a different layer and corresponding power supply pads formed on a pad forming layer of a multi-layered package substrate.

3. (Amended) A flip chip semiconductor device of a multi-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged outside of said power supply pads;

in which said input and output cells form input and output cell groups which in turn form columns of input and output cell groups extending in directions crossing peripheral edges of said pad forming layer.

11. (Amended) A flip chip semiconductor device of a multi-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged outside of said power supply pads;

in which said macro-cells are formed inside of said input and output cells.

IN THE DRAWINGS

Please find enclosed copies of the drawing sheets containing Figs. 3, 4, and 6, as originally filed, with proposed changes in red for the approval of the Examiner. In addition, please find enclosed proposed new Figs. 20 and 21 for the approval of the Examiner.

REMARKS

Claims 1 – 30 are currently pending in the application. Claims 9, 14 – 17, 20 – 23 and 25 – 30 are currently withdrawn from consideration. Applicant amends claims 2, 3 and 11.

OBJECTION TO DRAWINGS

The drawings are objected to under 37 C.F.R. § 1.83(a) and under 37 C.F.R. 1.84(p)(5) for failing to show every feature specified in the claims and for including reference sign(s) not mentioned in the description. Specifically, the Examiner finds that the drawings fail to show a multilayered structure having cell and pad forming layers, and having macro-cells and that the drawings show reference sign 121 not mentioned in the description. Applicant attaches proposed red-line changes to Figs. 3 and 6 and new Figs.